AMENDMENTS

In the Claims

41. A semiconductor processing method of forming a conductive transistor gate over a substrate comprising:

forming a conductive gate electrode over a gate dielectric layer on a substrate, the gate electrode having sidewalls and an interface with the gate dielectric layer;

forming sidewall spacers comprising nitride on the gate electrode's sidewalls, the sidewall spacers joining with the gate dielectric layer; and

after forming the sidewall spacers comprising nitride, exposing the substrate to oxidizing conditions effective to channel oxidants through the gate dielectric layer and underneath the sidewall spacers joined therewith, wherein a portion of the gate electrode, laterally adjacent the sidewall spacers and at the interface with the gate dielectric layer, is oxidized.

43. The method of claim 41, wherein the gate electrode comprises a first conductive layer a portion of which defines the interface, an overlying metal layer, and an electrically conductive reaction barrier layer interposed between the first layer and the overlying layer.

44. The method of claim 41, wherein the forming of the sidewall spacers includes:

depositing a first material over the gate electrode;

depositing a second material over the first material; and

anisotropically etching the first and second materials to a degree sufficient to leave the spacers over the gate's sidewalls, the spacers being defined by both the first and second material.

45. A semiconductor processing method of forming a conductive gate comprising:

forming a conductive gate structure on a first layer which is disposed on a substrate, the gate structure comprising a gate electrode having sidewalls and an interface with the first layer;

forming sidewall spacers laterally adjacent the conductive gate structure's sidewalls sufficiently to cover all conductive material comprising the sidewalls, the sidewall spacers comprising an oxidation resistant material; and

after forming the oxidation resistant sidewall spacers, conducting an oxidizing step by channeling oxidants through the first layer which is outwardly exposed laterally proximate the oxidation resistant sidewall spacers wherein the oxidation resistant sidewall spacers provide that only a portion of the gate electrode, adjacent the oxidation resistant sidewall spacers and at the interface with the first layer, is oxidized.

46. The method of claim 45, wherein the layer through which oxidants are channeled comprises a gate dielectric layer.

47. The method of claim 45, wherein the gate structure comprises polysilicon layer, an overlying metal layer, and an electrically conductive reaction barrier layer intermediate the polysilicon layer and the overlying metal layer.

48. The method of claim 45, wherein the forming of the sidewall spacers comprises:

depositing a first material over the gate structure;

depositing a second material over the first material; and

anisotropically etching the first and second materials to a degree sufficient to leave the sidewall spacers over the gate structure's sidewalls.

49. The method of claim 45, wherein the forming of the sidewall spacers comprises:

depositing a first material over the gate structure;

anisotropically etching the first material to a degree sufficient to leave first sidewall spacers over the gate structure;

depositing a second material over the first sidewall spacers; and

anisotropically etching the second material to a degree sufficient to leave second sidewall spacers over the first sidewall spacers.

50. A semiconductor processing method of forming a conductive transistor gate over a substrate comprising:

forming a dielectric layer on a substrate;

forming a conductive gate structure over the dielectric layer, the gate structure having sidewalls defining a lateral dimension of the gate structure;

forming non-oxide material over the gate structure and the dielectric layer;

anisotropically etching the non-oxide material to form spacers on the sidewalls, the spacers laterally adjacent the gate structure and joining with the gate dielectric layer thereat; and

exposing the substrate to oxidizing conditions effective to oxidize only that portion of the gate structure adjacent the spacers and the dielectric layer.

51. The method of claim 50, wherein the forming of the non-oxide material and the anisotropically etching thereof comprises:

depositing a first non-oxide material over the gate structure;

anisotropically etching the first non-oxide material to a degree sufficient to leave first spacers over the gate structure sidewalls;

depositing a second non-oxide material over the first spacers; and

anisotropically etching the second non-oxide material to a degree sufficient to leave second spacers over the first spacers.

52. A semiconductor processing method of forming a conductive gate comprising:

forming a gate structure atop a substrate having a dielectric layer thereon, at least a portion of the gate structure being conductive, the conductive portion comprising:

a polysilicon layer,

an overlying metal, and

a reaction barrier layer interposed between the polysilicon and the overlying metal;

covering a top and sidewalls of the gate structure with an oxidation resistant material, said covering comprising:

a first barrier material contacting the sidewalls, and

a second barrier material disposed over the first barrier material,

anisotropically etching the oxidation resistant material to a degree sufficient to leave the oxidation resistant material laterally adjacent to and covering all of the sidewalls of the gate structure while exposing the dielectric layer adjacent the gate structure; and

exposing the substrate to oxidation conditions effective to oxidize a portion of the gate structure laterally adjacent the covered sidewalls and adjacent the dielectric layer.

53. A semiconductor processing method of forming a conductive gate comprising:

forming a gate structure atop a substrate having a dielectric layer thereon, at least a portion of the gate structure being conductive, the conductive portion comprising:

a polysilicon layer,

an overlying metal, and

a reaction barrier layer interposed between the polysilicon and the overlying metal;

covering a top and sidewalls of the gate structure with an oxidation resistant material, said covering comprising:

a first barrier material contacting the sidewalls, and

a second barrier material disposed over the first barrier material,

anisotropically selectively etching the oxidation resistant material relative to the dielectric layer to a degree sufficient to leave the oxidation resistant material laterally adjacent to and covering all of the sidewalls of the gate structure while exposing the dielectric layer adjacent the gate structure; and

conducting an oxidizing step by channeling oxidants through the dielectric layer which is outwardly exposed laterally proximate the oxidation resistant material wherein the oxidation resistant material

provides that only a portion of the gate structure, adjacent the oxidation resistant material and at the interface with the dielectric layer, is oxidized.

New Claims

54. A semiconductor processing method of forming a conductive transistor gate over a substrate comprising:

forming a conductive gate over a gate dielectric layer on a monocrystalline silicon substrate, the gate having sidewalls which join with the gate dielectric layer and the gate further having an interface with the gate dielectric layer;

forming a first nitride containing material over the substrate and gate to a thickness ranging from between 50 to 500 Angstroms;

anisotropically etching the first nitride containing material to a degree sufficient to leave first sidewall spacers over the respective entireties of the gate sidewalls, the spacers joining with the gate dielectric layer and having respective outwardly exposed sidewall surfaces;

forming a second nitride containing material over the substrate and outwardly exposed sidewalls surfaces of the first sidewall spacers;

anisotropically etching the second nitride containing material to a degree sufficient to leave second sidewall spacers respectively over the outwardly exposed sidewall surfaces of the first sidewall spacers, the second sidewall spacers completely covering exposed sidewall surfaces of the first sidewall spacers; and

after the etching of the second nitride containing material and with no portion of the gate being exposed, exposing the substrate to oxidizing conditions effective to oxidize at least a portion of the gate interface with the gate dielectric layer by channeling oxidants through the gate dielectric

layer, said oxidants entering the gate dielectric layer through exposed portions thereof and being channeled underneath both the first and second sidewall spacers.

55. A semiconductor processing method of forming a conductive transistor gate over a substrate comprising:

forming a conductive gate electrode over a gate dielectric layer on a substrate, the gate electrode having sidewalls and an interface with the gate dielectric layer;

forming sidewall spacers comprising nitride adjoining the gate electrode's sidewalls, the sidewall spacers joining with the gate dielectric layer; and

after forming the sidewall spacers comprising nitride, exposing the substrate to oxidizing conditions effective to channel oxidants through the gate dielectric layer and underneath the sidewall spacers joined therewith, wherein a portion of the gate electrode, laterally adjacent the sidewall spacers and at the interface with the gate dielectric layer, is oxidized.

56. The method of claim 55, wherein forming the gate electrode comprises forming a first conductive layer a portion of which defines the interface, forming an electrically conductive reaction barrier layer atop the first conductive layer and forming an overlying metal layer.

57. The method of claim 55, wherein forming the sidewall spacers includes:

depositing a first material over the gate electrode;

depositing a second material over the first material; and

anisotropically etching the first and second materials to a degree sufficient to leave the spacers over the gate's sidewalls, the spacers being defined by both the first and second material.

58. A semiconductor processing method of forming a conductive gate comprising:

forming a conductive gate structure on a first layer which is disposed on a substrate, the gate structure comprising a gate electrode having sidewalls and an interface with the first layer;

forming sidewall spacers laterally abutting the conductive gate structure's sidewalls sufficiently to cover all conductive material comprising the sidewalls, the sidewall spacers comprising an oxidation resistant material; and

after forming the oxidation resistant sidewall spacers, oxidizing by channeling oxidants through the first layer which is outwardly exposed laterally proximate the oxidation resistant sidewall spacers wherein the oxidation resistant sidewall spacers provide that only a portion of the gate electrode, adjacent the oxidation resistant sidewall spacers and at the interface with the first layer, is oxidized.

59. The method of claim 58, wherein oxidizing comprises channeling oxidants through a gate dielectric layer.

60. The method of claim 58, wherein forming the gate structure comprises forming a polysilicon layer, forming an electrically conductive reaction barrier layer atop the polysilicon and forming an overlying metal layer.

61. The method of claim 58, wherein forming sidewall spacers comprises:

depositing a first material over the gate structure;

depositing a second material over the first material; and

anisotropically etching the first and second materials to a degree sufficient to leave the sidewall spacers over the gate structure's sidewalls.

62. The method of claim 58, wherein forming sidewall spacers comprises:

depositing a first material over the gate structure;

anisotropically etching the first material to a degree sufficient to leave first sidewall spacers over the gate structure;

depositing a second material over the first sidewall spacers; and

anisotropically etching the second material to a degree sufficient to leave second sidewall spacers over the first sidewall spacers.

63. A semiconductor processing method of forming a conductive transistor gate over a substrate comprising:

forming a conductive gate over a gate dielectric layer on a substrate, the gate having sidewalls which join with the gate dielectric layer and the gate having an interface with the gate dielectric layer, the gate including a metal nitride layer;

forming nitride containing spacers abutting the respective entireties of the gate sidewalls, the spacers joining with the gate dielectric layer; and

after forming the spacers, exposing the substrate to oxidizing conditions effective to oxidize at least a portion of the gate interface with the gate dielectric layer.

64. The method of claim 63, wherein forming the gate structure comprises forming a first conductive layer a portion of which defines the interface, forming an electrically conductive reaction barrier layer atop the first conductive layer and forming an overlying metal layer.

65. The method of claim 63, wherein forming the gate structure comprises forming a polysilicon layer, forming an electrically conductive reaction barrier layer atop the polysilicon layer and forming an overlying metal layer.

66. The semiconductor processing method of claim 63, wherein forming the nitride containing spacers includes:

depositing a first nitride containing material over the gate;

depositing a second nitride containing material over the first nitride containing material; and

anisotropically etching the first and second nitride containing materials to a degree sufficient to leave the spacers over the gate sidewalls, the spacers being defined by both first and second nitride containing material.

67. The semiconductor processing method of claim 63, wherein forming the nitride containing spacers includes:

depositing a first nitride containing material over the gate;

anisotropically etching the first nitride containing material to a degree sufficient to leave first nitride containing spacers over the gate sidewalls;

depositing a second nitride containing material over the first nitride containing spacers; and

anisotropically etching the second nitride containing material to a degree sufficient to leave second nitride containing spacers proximate the first nitride containing spacers.

68. The semiconductor processing method of claim 63, including:

depositing a first nitride containing material over the gate;

anisotropically etching the first nitride containing material to a degree sufficient to leave first nitride containing spacers over the gate sidewalls; and further comprising after the exposing of the substrate to the oxidizing conditions:

depositing a second nitride containing material over the first nitride containing spacers; and

anisotropically etching the second nitride containing material to a degree sufficient to leave second nitride containing spacers proximate the first nitride containing spacers.

69. The semiconductor processing method of claim 63, wherein the gate includes a gate top and further comprising, prior to exposing the substrate to the oxidizing conditions, forming an oxidation resistant material over the gate top which, together with the nitride containing spacers, effectively encapsulates the gate.

70. The semiconductor processing method of claim 63, wherein the gate includes a gate top and further comprising, prior to exposing the substrate to the oxidizing conditions, forming an nitride containing oxidation resistant material over the gate top which, together with the nitride containing spacers, effectively encapsulates the gate.